Properties of Perfect Computer Memory

unlimited capacity

instant random access

unlimited bandwidth for sequential access

for free

persistent, always, for ever
The Storage Hierarchy

Memory

cpu

Registers

core

L1

L2

L3

main memory

flash/hard disk

capacity, access time

costs/Byte, bandwidth

inclusion
Typical Access Times

- **core**
  - Registers
  - L1
  - L2
  - L3
  - main memory
  - flash/hard disk

Access times:
- 1 cycle (1cyc)
- 4 cycles (4cyc)
- 10 cycles (10cyc)
- 60 cycles (60cyc)
- 60 nanoseconds (60ns)
- 5 milliseconds (5ms)
Relative Distances!

“L1 cache is like grabbing a piece of paper from your desk (2 second),

L2 cache is picking up a book from a nearby shelf (5 seconds),

L3 cache is picking up a book from the next room (30 seconds),

DRAM is taking a walk down the hall to buy a Twix bar (90 seconds).“
“hard disk is like walking from Saarland to Hawaii."

7,500,000 seconds of walking!

= 86.8 days!
Relative Sizes!

L1

L2

L3

DRAM

Factor 8

Factor 256

Factor 524,288
Tasks of **Each** Level

- localization of data objects
- caching of data from lower level: inclusion (usually)
- data replacement strategies
- writing modified data (write through vs write back)
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This leads to **The All Levels are Equal Pattern**.
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Twix analogy inspired from:
http://duartes.org/gustavo/blog/post/what-your-computer-does-while-you-wait
[retrieved Nov 8, 2013]
yet: I extended the analogy a bit

Cache latency numbers are based on this article:
Performance Analysis Guide for Intel® Core™ i7 Processor and Intel® Xeon™ 5500 processors
By Dr David Levinthal PhD. Version 1.0
[retrieved Nov 8, 2013]