A Single-Core Storage Hierarchy

core
  Registers
  L1
  L2
  L3
  main memory
  flash/hard disk

capacity, access time
costs/Byte, bandwidth
A Single-Core Storage Hierarchy

- CPU
  - core
  - Registers
  - L1
  - L2
  - L3

- main memory
- flash/hard disk

- capacity, access time
- costs/Byte, bandwidth
Non-Uniform Memory Access (NUMA)

CPU with levels of cache (L1, L2, L3) connected to main memory. The diagram shows the time delays for accessing different levels of memory.

- Accessing L1 cache: 60 ns
- Accessing L2 cache: ~700 ns

The main memory is connected to flash/hard disk.
Cache latency numbers are based on this article:
Performance Analysis Guide for Intel® CoreTM i7 Processor and Intel® XeonTM 5500 processors
By Dr David Levinthal PhD. Version 1.0
[retrieved Nov 8, 2013]